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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/645,027	08/21/2003	Shahla Khorram	BP 2973	7363

34399 7590 09/25/2007

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EXAMINER	
HOANG, ANN THI	
ART UNIT	**PAPER NUMBER**
2836	

MAIL DATE	DELIVERY MODE
09/25/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/645,027	KHORRAM, SHAHLA	
	Examiner	Art Unit	
	Ann T. Hoang	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 May 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 4-16, 19 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Woo et al. (US 6,445,039) in view of Yue et al. (6,597,227) and Tsuji (US 5,901,023).

Regarding claim 1, Woo et al. discloses a radio frequency integrated circuit (RFIC) having sectional electrostatic discharge (ESD) protection, the RFIC comprising:

an analog receive section 3402 operably coupled to convert inbound radio frequency (RF) signals 3410 into inbound low intermediate frequency (IF) signals 3412; and

a digital section 3416 operably coupled to convert the inbound low IF signals 3412 into inbound digital data 3414.

Fig. 34 and column 39, lines 40-45 describe these elements with their numerical references. Additionally, Woo et al. discloses in column 39, lines 57-63 that the RFIC may also contain an analog transmit section, which would be operably coupled to convert outbound low IF signals into outbound RF signals, to compliment analog receive section 3402, thereby making the RFIC a transceiver system. For two-way

transmission, digital section 3416 would necessarily convert outbound digital data into the outbound low IF signals as well. See column 58, lines 42-52 and column 61, lines 62-67.

Woo et al. also discloses RFIC sections (6102, 6104, 6106) to have localized ground connections (6110, 6112, 6114) as well as localized ESD protection circuitry 6108, with each local ESD protection circuit operably coupled to its respective local ground connection. See Fig. 61; column 2, lines 3-9; column 63, lines 14-19 and 60-67; and line 64, lines 1-18. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to provide localized ground connections and ESD protection circuitry to the analog receive, analog transmit, and digital sections, which are the major different sections of the RFIC, in order to minimize noise injection while preventing ESD damage. In this arrangement, analog receive section 3402 has an analog receive ground connection and includes analog receive ESD protection circuitry operably coupled to the analog receive ground connection; the analog transmit section would have an analog transmit ground connection and include analog transmit ESD protection circuitry operably coupled to the analog transmit ground connection; and digital section 3416 would have a digital ground connection.

Woo et al. does not disclose a first inductor assembly operably coupling the analog receive ground connection to the digital ground connection or a second inductor assembly operably coupling the analog transmit ground connection to the digital ground connection.

However, Yue et al. discloses connecting inductor assemblies (110, 110a) in series with ESD protection circuitry (40, 40a) to reduce the adverse affects caused by parasitic capacitance of the ESD protection circuitry (40, 40a). See abstract; Fig. 9; and column 2, lines 45-56. It would have been obvious to one of ordinary skill in the art at the time of the invention to include a first inductor assembly and a second inductor assembly, as suggested by Yue et al., connected in series with the analog receive ESD protection circuitry and analog transmit ESD protection circuitry, respectively, in the RFIC of Woo et al. in order to reduce the adverse affects caused by parasitic capacitances of the analog receive and analog transmit ESD protection circuitry. Yue et al. does not disclose placing inductor assemblies between different ground connections. Rather, the reference discloses placing the inductor assemblies between a main circuit and a voltage rail.

However, Tsuji discloses a desire to provide ESD protection circuitry between analog 11 and digital (14, 15) domains of an IC in order to reduce the effects of noise that analog domains receive from digital domains. Furthermore, Tsuji discloses connecting the ESD protection circuitry across analog ground and digital ground connections. See Figs. 1, 4 and 5; column 1, lines 67-68; column 2, lines 1-3 and 20-25; and column 3, lines 16-17 and 32-36. Since the inductors of Yue et al. would serve as ESD protection between analog and digital domains if placed between the different ground connections, it would have been obvious to one of ordinary skill in the art at the time of the invention to place the inductors of Yue et al. between different ground connections in the RFIC of Woo et al. so that the inductors could be used for a dual

purpose: to reduce the adverse affects caused by parasitic capacitances of the analog receive and analog transmit ESD protection circuitry, since they would still be in a series connection with the ESD protection circuitry, and to provide ESD protection between analog and digital domains. This configuration would result in a first inductor assembly operably coupling the analog receive ground connection to the digital ground connection and a second inductor assembly operably coupling the analog transmit ground connection to the digital ground connection.

Regarding claim 4, Woo et al. discloses multiple RFIC sections (6102, 6104, 6106). These sections are labeled for the purpose of an example drawing, the function of each unspecified, and it is understood that any number of RFIC sections may be utilized. See Fig. 61 and column 64, lines 16-18. Woo et al. shows RFIC sections (6102, 6104, 6106) to each have a second ESD protection circuit operably coupled to a localized power source connection (6110, 6112, 6114). The multiple RFIC sections (6102, 6104, 6106) are interpreted to include analog receive section 3402, the analog transmit section, and digital section 3416. See above rejection on claim 1. Thus:

analog receive section 3402 includes second analog receive ESD protection circuitry operably coupled to an analog receive power source connection;

the analog transmit section includes second analog transmit ESD protection circuitry operably coupled to an analog transmit power source connection; and

digital section 3416 includes a digital power source connection.

Woo et al. does not disclose a third inductor assembly operably coupling the analog receive power source connection to the digital power source connection or a

fourth inductor assembly operably coupling the analog transmit power source connection to the digital power source connection.

However, Yue et al. discloses connecting inductor assemblies (110, 110a) in series with ESD protection circuitry (40, 40a) to reduce the adverse affects caused by parasitic capacitance of the ESD protection circuitry (40, 40a). See abstract; Fig. 9; and column 2, lines 45-56. It would have been obvious to one of ordinary skill in the art at the time of the invention to include a first inductor assembly and a second inductor assembly, as suggested by Yue et al., connected in series with the analog receive ESD protection circuitry and analog transmit ESD protection circuitry, respectively, in the RFIC of Woo et al. in order to reduce the adverse affects caused by parasitic capacitances of the analog receive and analog transmit ESD protection circuitry. Yue et al. does not disclose placing inductor assemblies between different power source connections. Rather, the reference discloses placing the inductor assemblies between a main circuit and a voltage rail.

However, Tsuji discloses a desire to provide ESD protection circuitry between analog 11 and digital (14, 15) domains of an IC in order to reduce the effects of noise that analog domains receive from digital domains. Furthermore, Tsuji discloses connecting the ESD protection circuitry across analog power and digital power connections. See Figs. 1, 4 and 5; column 1, lines 67-68; column 2, lines 1-3 and 20-25; and column 3, lines 16-17 and 32-36. Since the inductors of Yue et al. would serve as ESD protection between analog and digital domains if placed between the different power connections, it would have been obvious to one of ordinary skill in the art at the

time of the invention to place the inductors of Yue et al. between different power connections in the RFIC of Woo et al. so that the inductors could be used for a dual purpose: to reduce the adverse affects caused by parasitic capacitances of the analog receive and analog transmit ESD protection circuitry, since they would still be in a series connection with the ESD protection circuitry, and to provide ESD protection between analog and digital domains. This configuration would result in a third inductor assembly operably coupling the analog receive power source connection to the digital power source connection and a fourth inductor assembly operably coupling the analog transmit power source connection to the digital power source connection. See above rejection on claim 1.

Regarding claim 5, Woo et al. discloses:

a low noise amplifier 3502 operably coupled to amplify the inbound RF signals 3406 to produce amplifier inbound RF signals 3410;

a mixing module 1916 operably coupled to mix amplified inbound RF signals 3410 with a receive local oscillation 1902 to produce down converted signals 1918; and

a receive filtering module 1912 operably coupled to filter down converted signals 1918 to produce inbound low IF signals 3412.

The reference actually discloses a cascade of multiple mixers and filters which tune the received signal before signal processing circuitry splits the analog component off of the inbound low IF signal and outputs it in a digital format. From this, it is understood that the signal processing circuitry includes an analog to digital converter with an analog portion, as would be required for this type of splitting. See abstract;

Figs. 19, 34, and 35; column 60, lines 66-67 and column 61, lines 1-7. Some of these components are shown as connecting to but not within the block that represents analog receive section 3402 in the drawings. However, it would be obvious to one of ordinary skill in the art at the time of the invention to diagram them as being a part of analog receive section 3402, as they perform the same functions irregardless of their grouping in the drawings.

Since Woo et al. discloses an unlimited number of RFIC sections (6102, 6104, 6106) to have localized ground connections (6110, 6112, 6114) (see Fig. 61), it is interpreted that low noise amplifier 3502, mixing module 1916, receive filtering module 1912, and the analog portion of the analog to digital converter constitute RFIC sections and that these RFIC sections each have a localized ground connection. See above rejection on claim 1. Thus, low noise amplifier 3502 has a low noise amplifier ground connection, mixing module 1916 has a mixing module ground connection, receive filtering module 1912 has a receive filtering ground connection, and the analog portion has an analog portion ground connection.

Woo et al. does not disclose any inductors operably coupling the aforementioned ground connections.

However, Yue et al. discloses connecting inductor assemblies (110, 110a) in series with ESD protection circuitry (40, 40a) to reduce the adverse affects caused by parasitic capacitance of the ESD protection circuitry (40, 40a). See abstract; Fig. 9; and column 2, lines 45-56. Yue et al. does not disclose placing inductor assemblies

between different ground connections. Rather, the reference discloses placing the inductor assemblies between a main circuit and a voltage rail.

However, Tsuji discloses a desire to provide ESD protection circuitry between analog 11 and digital (14, 15) domains of an IC in order to reduce the effects of noise that analog domains receive from digital domains. Furthermore, Tsuji discloses connecting the ESD protection circuitry across analog ground and digital ground connections. See Figs. 1, 4 and 5; column 1, lines 67-68; column 2, lines 1-3 and 20-25; and column 3, lines 16-17 and 32-36. Since the inductors of Yue et al. would serve as ESD protection between different ground connections, it would have been obvious to one of ordinary skill in the art at the time of the invention to place the inductors of Yue et al. between different ground connections in the RFIC of Woo et al. so that the inductors could be used for a dual purpose: to reduce the adverse affects caused by parasitic capacitances of the analog receive and analog transmit ESD protection circuitry, since they would still be in a series connection with the ESD protection circuitry, and to provide ESD protection between different grounds and between analog and digital domains. This configuration would result in a first inductor operably coupling the low noise amplifier ground connection to the mixing module ground connection, a second inductor operably coupling the mixing module ground connection to the receive filtering ground connection, a third inductor operably coupling the receive filtering ground connection to the analog portion ground connection, and a fourth inductor operably coupling the analog portion ground connection to the digital ground connection. See above rejection on claim 1.

Regarding claim 6, Woo et al. discloses in column 39, lines 57-63 an analog transmit section with functionally equivalent circuitry as the analog receive section. It is understood that an analog transmit section would comprise:

a power amplifier operably coupled to amplify up converted signals to produce the outbound RF signals;

a mixing module operably coupled to mix filtered low IF signals with a transmit local oscillation to produce the up converted signals;

a filtering module operably coupled to filter the outbound low IF signals to produce the filtered low IF signals; and

an analog portion of a digital to analog converter which converts digital outbound low IF signals into the outbound low IF signals.

These components would be the compliment of those in the analog receive section as described above. These components are also interpreted to constitute some of the RFIC sections (6102, 6104, 6106) with localized ground connections (6110, 6112, 6114). See above rejection on claim 1. Woo does not disclose any inductors operably coupling the aforementioned ground connections.

However, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the method of inserting an inductor between different ground connections, as taught by Yue et al. and Tsuji, with the RFIC of Woo et al. in order to provide inductors used for a dual purpose: to reduce the adverse affects caused by parasitic capacitances of the analog receive and analog transmit ESD protection circuitry, since they would still be in a series connection with the ESD protection

circuitry, and to provide ESD protection between different grounds and between analog and digital domains. Claim 6 is rejected under the same reasoning as that of claim 5. See above rejection.

Regarding claim 7, Woo et al. discloses:

a low noise amplifier 3502 operably coupled to amplify inbound RF signals 3406 to produce amplifier inbound RF signals 3410; and

an analog receive radio section (Fig. 19) operably coupled to convert amplified inbound RF signals 3410 into inbound low IF signals 3412.

These sections are interpreted to constitute some of the RFIC sections (6102, 6104, 6106) with localized ground connections (6110, 6112, 6114). See above rejection on claim 1. Some of these components are shown as connecting to but not within the block that represents analog receive section 3402 in the drawings. However, it would be obvious to one of ordinary skill in the art at the time of the invention to diagram them as being a part of analog receive section 3402, as they perform the same functions irregardless of their grouping in the drawings. Woo does not disclose any inductors operably coupling the aforementioned ground connections.

However, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the method of inserting an inductor between different ground connections, as taught by Yue et al. and Tsuji, with the RFIC of Woo et al. in order to provide inductors used for a dual purpose: to reduce the adverse affects caused by parasitic capacitances of the analog receive and analog transmit ESD protection circuitry, since they would still be in a series connection with the ESD protection

circuitry, and to provide ESD protection between different grounds and between analog and digital domains. Claim 7 is rejected under the same reasoning as that of claim 5. See above rejection.

Regarding claim 8, Woo et al. discloses in column 39, lines 57-63 an analog transmit section with functionally equivalent circuitry as the analog receive section. It is understood that an analog transmit section would comprise:

a power amplifier operably coupled to amplify up converted signals to produce the outbound RF signals; and

an analog transmit radio section operably coupled to produce the up converted signals from the outbound low IF signals.

These components would be the compliment of those in the analog receive section as described above. These components are interpreted to constitute some of the RFIC sections (6102, 6104, 6106) with localized ground connections (6110, 6112, 6114). See above rejection on claim 1. Woo does not disclose any inductors operably coupling the aforementioned ground connections.

However, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the method of inserting an inductor between different ground connections, as taught by Yue et al. and Tsuji, with the RFIC of Woo et al. in order to provide inductors used for a dual purpose: to reduce the adverse affects caused by parasitic capacitances of the analog receive and analog transmit ESD protection circuitry, since they would still be in a series connection with the ESD protection circuitry, and to provide ESD protection between different grounds and between analog

and digital domains. Claim 8 is rejected under the same reasoning as that of claim 5. See above rejection.

Regarding claim 9, Woo et al. discloses a radio frequency integrated circuit (RFIC) having sectional electrostatic discharge (ESD) protection, the RFIC comprising:

an analog receive section 3402 operably coupled to convert inbound radio frequency (RF) signals 3410 into inbound low intermediate frequency (IF) signals 3412;

a power amplifier operably coupled to amplify up converted signals to produce the outbound RF signals;

an analog transmit radio section operably coupled to produce the up converted signals from the outbound low IF signals, as this section would be the compliment of the analog receive section as described above; and

a digital section 3416 operably coupled to convert inbound low IF signals 3412 into inbound digital data 3414 and to necessarily convert outbound digital data into the outbound low IF signals.

See Fig. 34. These components are interpreted to constitute some of the RFIC sections (6102, 6104, 6106) with localized ground connections (6110, 6112, 6114). See above rejection on claim 1. Woo et al. discloses RFIC sections (6102, 6104, 6106) to also include localized ESD protection circuitry 6108, with each local ESD protection circuit operably coupled to its respective local ground connection. See Fig. 61; column 2, lines 3-9; column 63, lines 14-19 and 60-67; and line 64, lines 1-18. Thus, it is understood that analog receive section 3402, the power amplifier, the analog transmit radio section, and digital section 3416 would have corresponding ESD protection

circuitry and ground connections. Woo does not disclose any inductors operably coupling the aforementioned ground connections for ESD protection between analog and digital domains.

However, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the method of inserting an inductor between different ground connections, as taught by Yue et al. and Tsuji, with the RFIC of Woo et al. in order to provide inductors used for a dual purpose: to reduce the adverse affects caused by parasitic capacitances of the analog receive and analog transmit ESD protection circuitry, since they would still be in a series connection with the ESD protection circuitry, and to provide ESD protection between different grounds and between analog and digital domains. Claim 9 is rejected under the same reasoning as that of claim 1. See above rejection.

Claim 10 is rejected under the same reasoning as that of claim 2. See above rejection.

Claim 11 is rejected under the same reasoning as that of claim 3. See above rejection.

Regarding claim 12, Woo et al. shows RFIC sections (6102, 6104, 6106) to each have a second ESD protection circuit operably coupled to a localized power source connection (6110, 6112, 6114). The multiple RFIC sections (6102, 6104, 6106) are interpreted to include analog receive section 3402, the power amplifier, and digital section 3416. Thus:

analog receive section 3402 would include second analog receive ESD protection circuitry operably coupled to an analog receive power source connection;

the power amplifier would include second power amplifier ESD protection circuitry operably coupled to a power amplifier power source connection; and

digital 3416 section would include a digital power source connection.

Woo does not disclose any inductors operably coupling the aforementioned power source connections for ESD protection between analog and digital domains.

However, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the method of inserting an inductor between different power connections, as taught by Yue et al. and Tsuji, with the RFIC of Woo et al. in order to provide inductors used for a dual purpose: to reduce the adverse affects caused by parasitic capacitances of the analog receive and analog transmit ESD protection circuitry, since they would still be in a series connection with the ESD protection circuitry, and to provide ESD protection between different power source connections and between analog and digital domains. Claim 12 is rejected under the same reasoning as that of claim 4. See above rejection.

Claim 13 is rejected under the same reasoning as that of claim 5. See above rejection.

Claim 14 is rejected under the same reasoning as that of claim 6. See above rejection. The "analog transmit radio section" of claim 9 is understood to be essentially the same as the "analog transmit section" of claim 1.

Claim 15 is rejected under the same reasoning as that of claim 7. See above rejection.

Regarding claim 16, Woo et al. discloses a radio frequency integrated circuit (RFIC) having sectional electrostatic discharge (ESD) protection, the RFIC comprising:

a power amplifier operably coupled to amplify up converted signals to produce the outbound RF signals;

an analog radio section 5818 operably coupled to convert inbound RF signals 3506 into inbound low IF signals 3412 and operably coupled to produce the up converted signals from outbound low IF signals; and

a digital section 3416 operably coupled to convert inbound low IF signals 3412 into inbound digital data 3414 and to convert outbound digital data into the outbound low IF signals.

See Figs. 34, 35, and 58; column 58, lines 42-52 and column 61, lines 62-67. These sections are interpreted to constitute some of the RFIC sections (6102, 6104, 6106) with localized ground connections (6110, 6112, 6114) and localized ESD protection circuitry 6108, with each local ESD protection circuit operably coupled to its respective local ground connection. See Fig. 61. Woo does not disclose any inductors operably coupling the aforementioned ground connections for ESD protection between analog and digital domains.

However, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the method of inserting an inductor between different ground connections, as taught by Yue et al. and Tsuji, with the RFIC of Woo et al. in order to

provide inductors used for a dual purpose: to reduce the adverse affects caused by parasitic capacitances of the analog receive and analog transmit ESD protection circuitry, since they would still be in a series connection with the ESD protection circuitry, and to provide ESD protection between different ground connections and between analog and digital domains. Claim 16 is rejected under the same reasoning as that of claim 1. See above rejection.

Claim 19 is rejected under the same reasoning as that of claim 12. See above rejection. The "analog radio section" of claim 19 is understood to be a two-way transceiver equivalent of the "analog receive section" of claim 12.

Regarding claim 20, Woo et al. discloses analog radio section 5818 to comprise:

a low noise amplifier 3502 operably coupled to amplify inbound RF signals 3406 to produce amplifier inbound RF signals 3410;

a receive mixing module 1916 operably coupled to mix amplified inbound RF signals 3410 with a receive local oscillation 1902 to produce down converted signals 1918; and

a receive filtering module 1912 operably coupled to filter down converted signals 1918 to produce inbound low IF signals 3412.

It is understood that the signal processing circuitry includes an ADC analog portion of an analog to digital converter, as would be required for splitting the analog component off of the inbound low IF signal and outputting it in a digital format. See above rejection on claim 5. Since Woo et al. discloses analog radio section 5818 to

contain an analog transmit section to compliment analog receive section 3402, it is understood that analog radio section 5818 also comprises:

a transmit mixing module operably coupled to mix filtered low IF signals with a transmit local oscillation to produce the up converted signals;

a transmit filtering module operably coupled to filter the outbound low IF signals to produce the filtered low IF signals; and

a DAC analog portion of a digital to analog converter, wherein the digital to analog converter converts digital outbound low IF signals into the outbound low IF signals, as these components would be the compliment of those in the analog receive section as described above.

These components are interpreted to constitute some of the RFIC sections (6102, 6104, 6106) with localized ground connections (6110, 6112, 6114). Woo does not disclose any inductors operably coupling the aforementioned ground connections.

However, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the method of inserting an inductor between different ground connections, as taught by Yue et al. and Tsuji, with the RFIC of Woo et al. in order to provide inductors used for a dual purpose: to reduce the adverse affects caused by parasitic capacitances of the analog receive and analog transmit ESD protection circuitry, since they would still be in a series connection with the ESD protection circuitry, and to provide ESD protection between different ground connections and between analog and digital domains. Claim 20 is rejected under the same reasoning as that of claim 1. See above rejection.

3. Claims 2, 3, 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Woo et al. (US 6,445,039) in view of Yue et al. (6,597,227) and Tsuji (US 5,901,023), as applied to claims 1 and 16 above, and further in view of Kluge et al. (US 2003/0183403).

Regarding claim 2, Woo et al. discloses the desire to fabricate all blocks of the transceiver on a single die, as partitioning more and more functionality into a single integrated circuit chip allows for considerable savings in component parts costs. See column 17, lines 59-62. This entails fabricating the analog receive section, the analog transmit section, and the digital section on a single die. The references do not disclose that the first and second inductor assemblies are off-chip with respect to the single die.

However, Kluge et al. discloses fabricating components of an RFIC on a single die, but that, in an application involving relatively large sized inductors, an inductor 3 can be manufactured off-chip. See page 4, paragraph 37. It would have been obvious to one of ordinary skill in the art at the time of the invention to manufacture the first and second inductor assemblies off-chip with respect to the single die in order to not add the bulk of large inductors to the single die.

Regarding claim 3, Kluge et al. discloses that inductor 3 may be packaged within the same package housing the single die. See page 4, paragraph 37. It would have been obvious to one of ordinary skill in the art at the time of the invention to package the first and second inductor assemblies within the same package housing the single die in order to contain the RFIC in a single package.

Claim 17 is rejected under the same reasoning as that of claim 2. See above rejection.

Claim 18 is rejected under the same reasoning as that of claim 3. See above rejection.

Response to Arguments

4. Applicant's arguments with respect to claims 1-20 have been considered but are moot in view of the new ground(s) of rejection. Yue et al. discloses connecting inductor assemblies in series with ESD protection circuitry in order to form a series resonance circuit that reduces the adverse affects caused by parasitic capacitance of the ESD protection circuitry.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ann T. Hoang, whose telephone number is 571-272-2724. The examiner can normally be reached Monday-Thursday and every other Friday, 8 a.m. to 6 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Sherry, can be reached at 571-272-2084. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

ATH
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9/17/07

MICHAEL SHERRY
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